PHB/PHD66NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 06 — 2 August 2004 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Low on-state resistance.

1.3 Applications

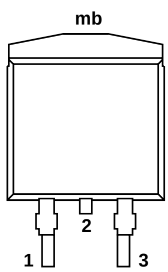
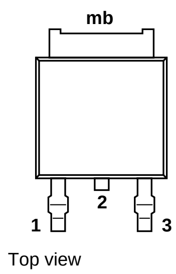
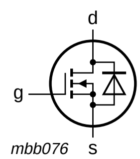
- DC-to-DC converters
- General purpose switching.

1.4 Quick reference data

- $V_{DS} \leq 25$ V
- $R_{DSon} \leq 10.5$ mΩ
- $I_D \leq 66$ A
- $Q_{gd} = 3.6$ nC (typ).

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate (g)	 SOT404 (D^2-PAK)  SOT428 (D-PAK)	
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		

[1] It is not possible to make a connection to pin 2 of the SOT404 and SOT428 packages.

PHILIPS

3. Ordering information

Table 2: Ordering information

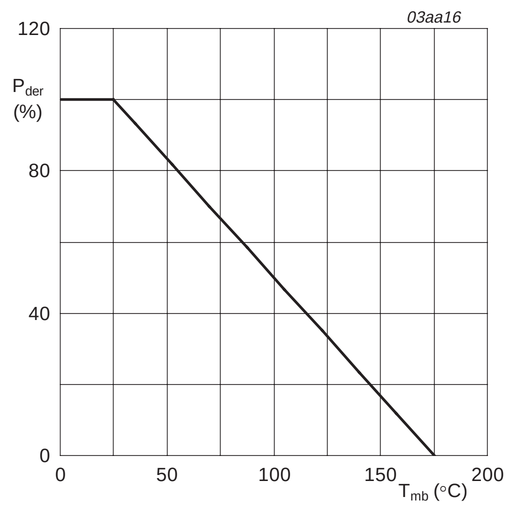
Type number	Package		
	Name	Description	Version
PHB66NQ03LT	D^2-PAK	Plastic single-ended surface mounted package (Philips version of D^2-PAK); 3 leads (one lead cropped)	SOT404
PHD66NQ03LT	D-PAK	Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 3: Limiting values

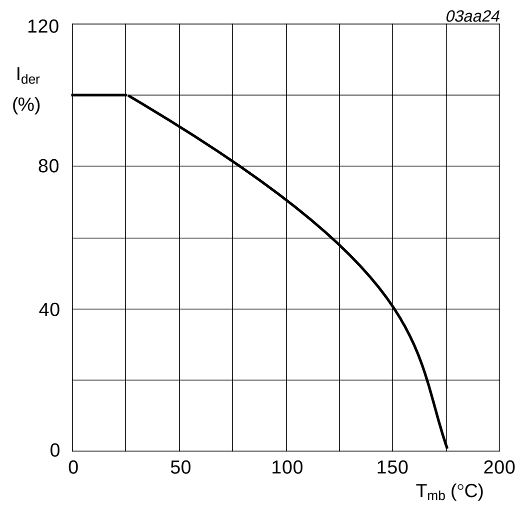
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	25	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	-	57	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	-	40	A
		T_{mb} = 25 °C; V_{GS} = 10 V	-	66	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	45	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	228	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	93	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	57	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	228	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 43 A; t_p = 0.15 ms; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	90	mJ



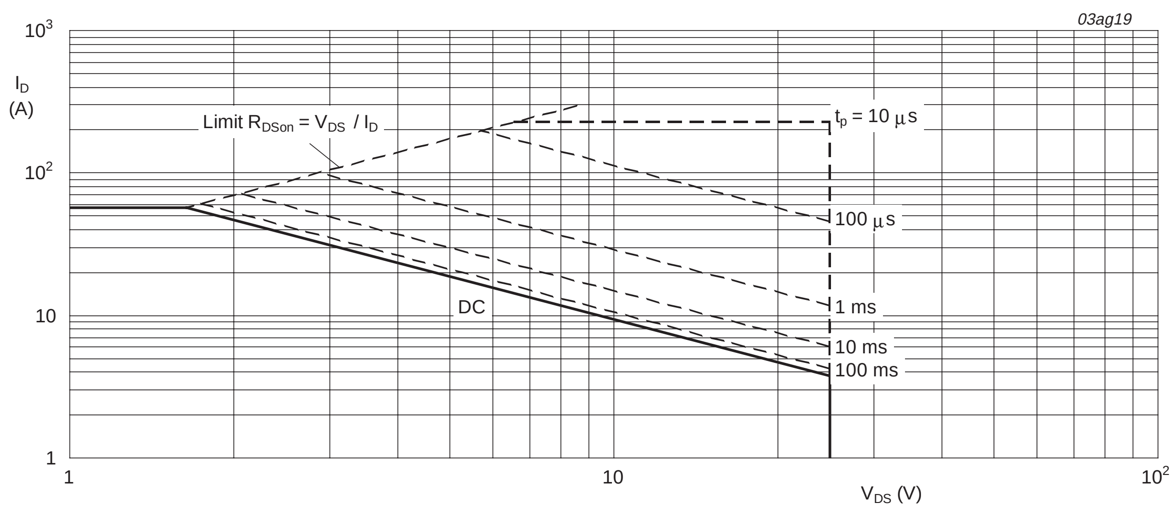
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25\ °C$; I_{DM} is single pulse; $V_{GS} = 5\ V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT404	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
	SOT428	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	75	-	K/W
		mounted on a printed-circuit board; SOT404 minimum footprint; vertical in still air	-	50	-	K/W

5.1 Transient thermal impedance

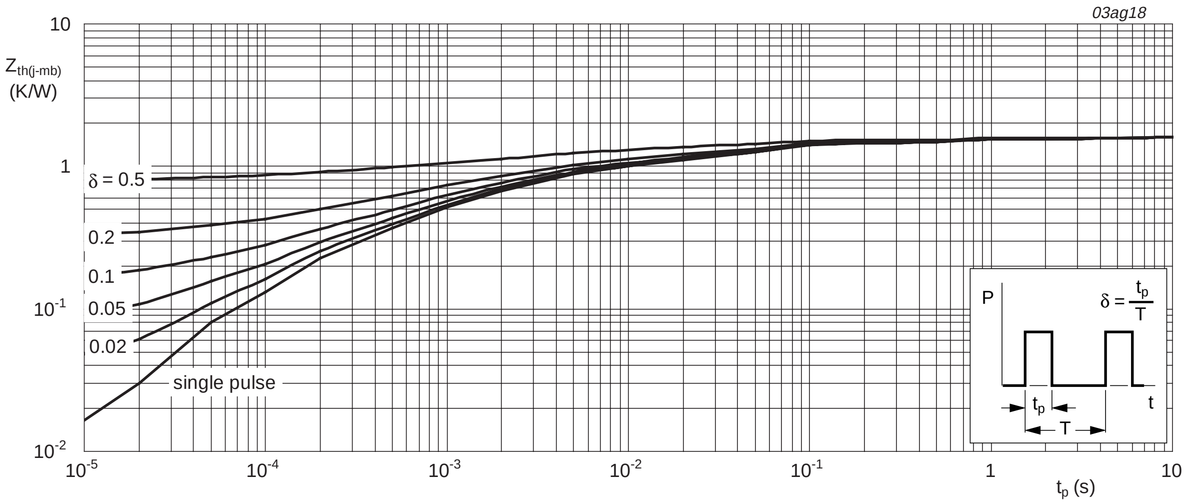


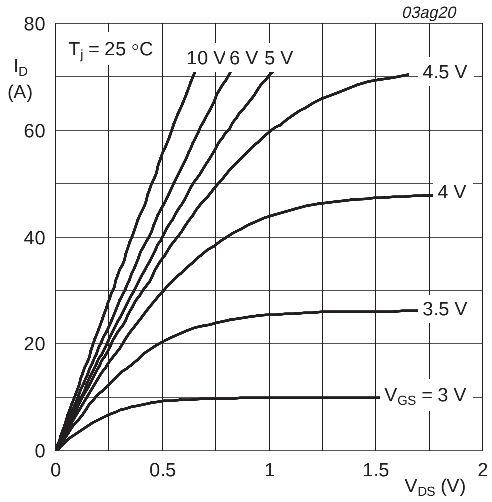
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

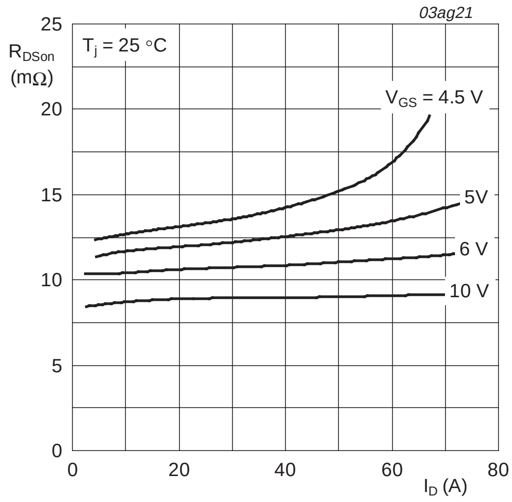
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	25	-	-	V
		T_j = –55 °C	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 25 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; Figure 6 and 8				
		T_j = 25 °C	-	9.1	10.5	mΩ
		T_j = 175 °C	-	16.4	18.9	mΩ
		V_{GS} = 5 V; I_D = 25 A; Figure 6 and 8	-	11.2	13.6	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 50 A; V_{DS} = 15 V; V_{GS} = 5 V; Figure 11	-	12	-	nC
Q_{gs}	gate-source charge		-	4.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 13	-	860	-	pF
C_{oss}	output capacitance		-	330	-	pF
C_{rss}	reverse transfer capacitance		-	145	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 5 V; R_G = 5.6 Ω	-	15	25	ns
t_r	rise time		-	90	135	ns
$t_{d(off)}$	turn-off delay time		-	25	40	ns
t_f	fall time		-	25	40	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 12	-	0.95	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 25 V	-	32	-	ns
Q_r	recovered charge		-	20	-	nC



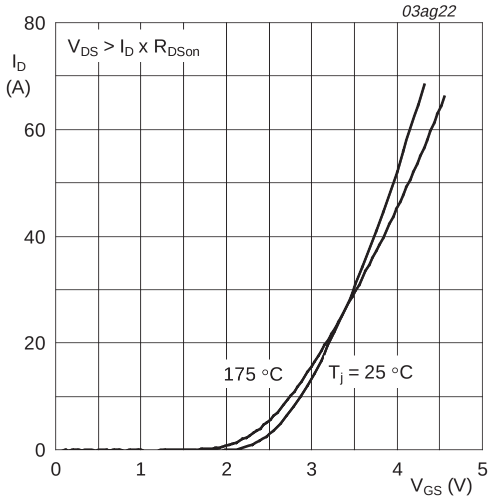
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



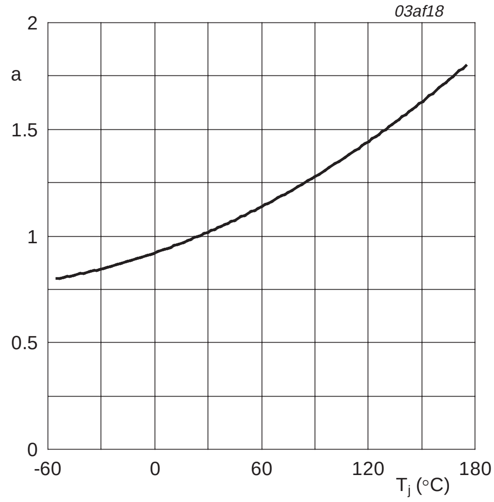
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



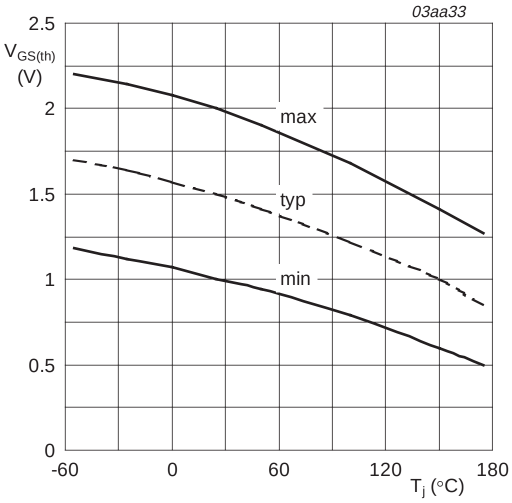
T_j = 25 °C and 175 °C; V_{DS} > I_D x R_{DSon}

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



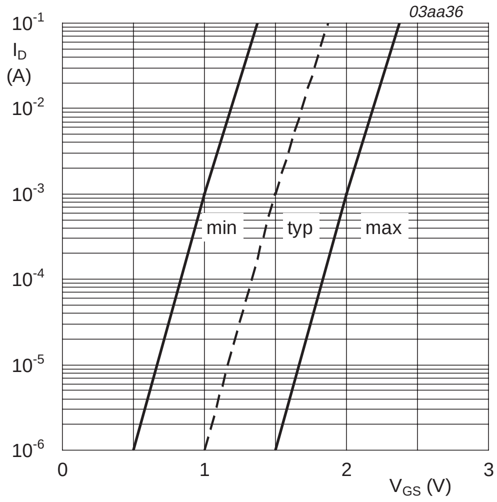
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



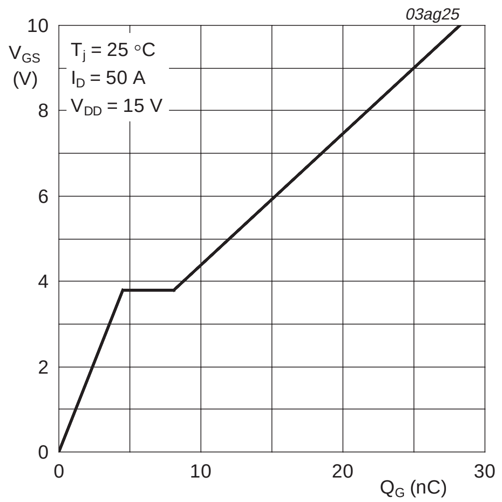
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



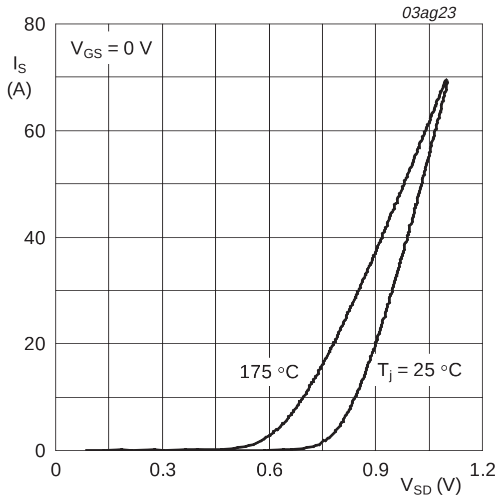
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



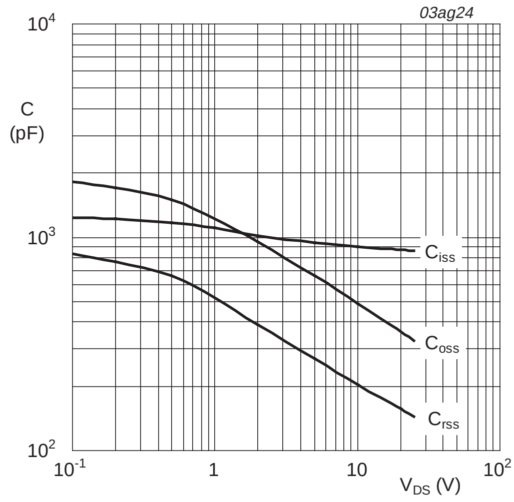
I_D = 50 A; V_{DS} = 15 V

Fig 11. Gate-source voltage as a function of gate charge; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



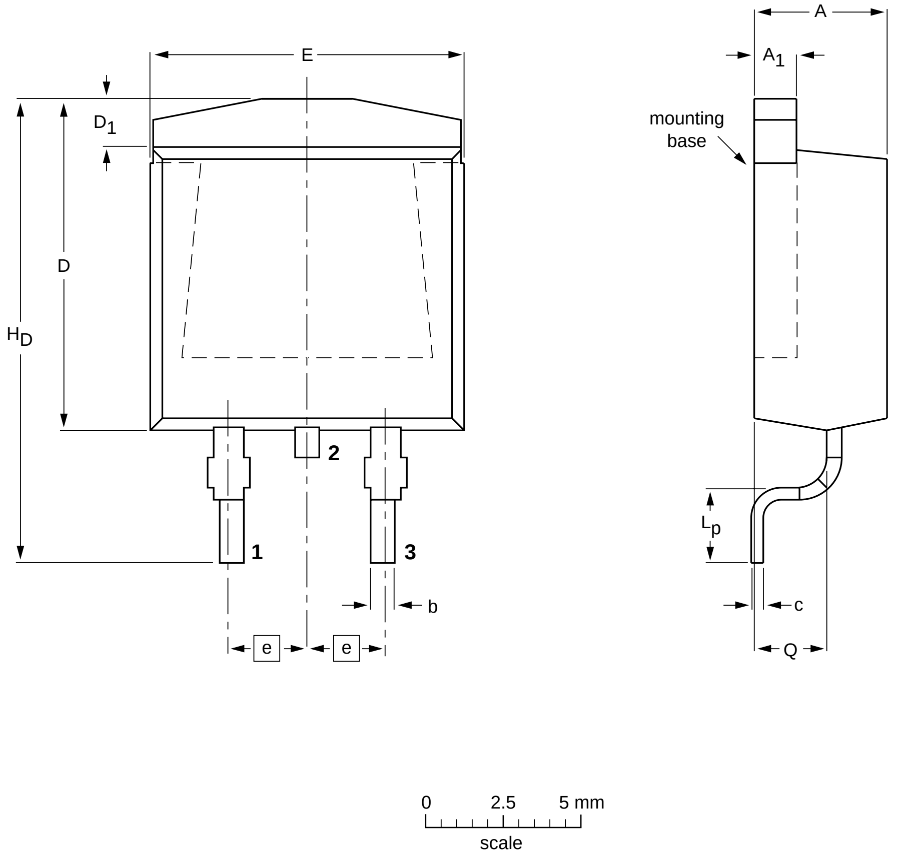
V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version of D2-PAK); 3 leads (one lead cropped)

SOT404



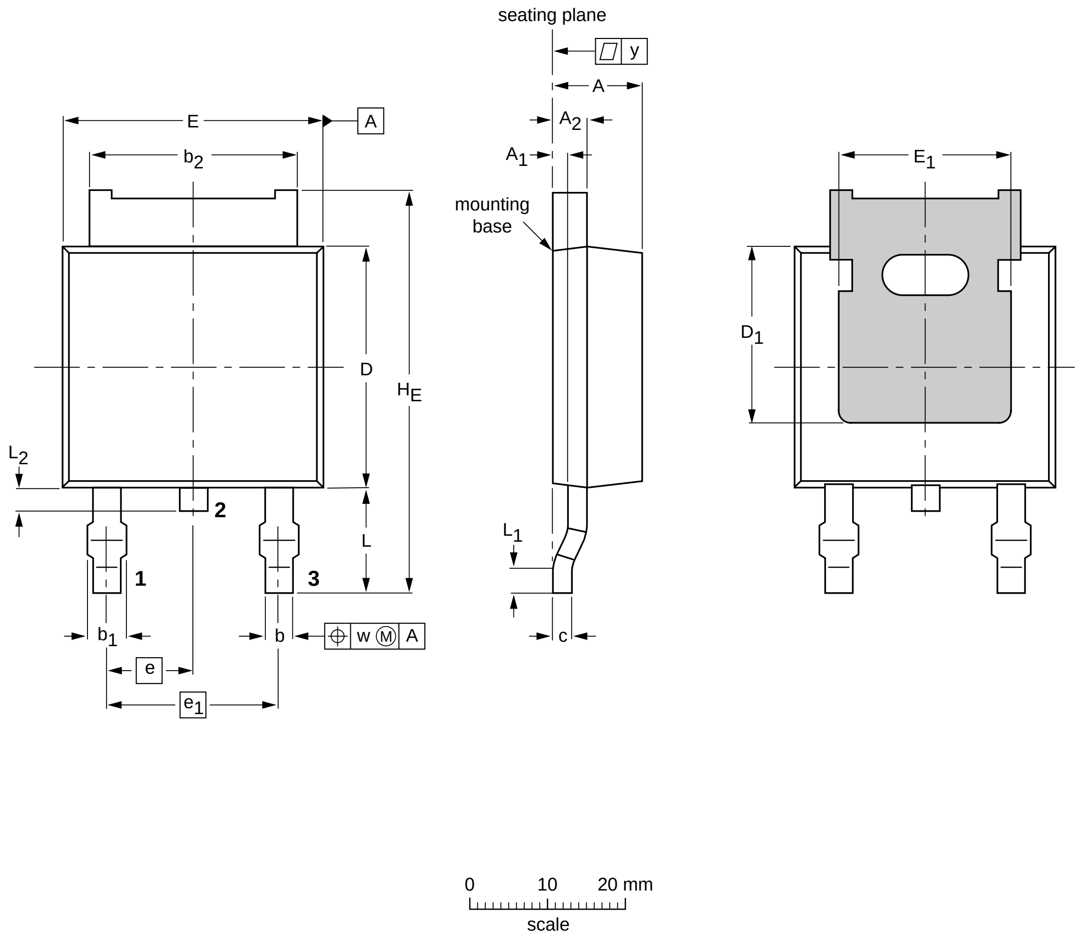
DIMENSIONS (mm are the original dimensions)

UNIT	A	A1	b	c	D max.	D1	E	e	Lp	HD	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						~~99-06-25~~ 01-02-12

Fig 14. SOT404 (D^2-PAK) package outline.

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1(1)	A_2	b	b_1	b_2	c	D	D_1 min.	E	E_1	e	e_1	H_E	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.26	0.4 0.2	6.22 5.98	4.0	6.73 6.47	4.81 4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~99-09-13~~ 01-12-11

Fig 15. SOT428 (D-PAK) package outline.

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Document number	Supersedes
PHB_PHD66NQ03LT_6	20040802	Product data sheet	-	9397 750 13429	PHP_PHB_PHD66NQ03LT_5
Modifications:	• Removal of PHP66NQ03LT (now in separate data sheet) • Data sheet updated to latest standard.				
PHP_PHB_PHD66NQ03LT_5	20040415	Product data sheet	-	9397 750 13107	PHP_PHB_PHD66NQ03LT_4
PHP_PHB_PHD66NQ03LT_4	20020909	Product data sheet	-	9397 750 10158	PHP_PHB_PHD66NQ03LT_3
PHP_PHB_PHD66NQ03LT_3	20020312	Product data sheet	-	9397 750 09284	PHP_PHB_PHD66NQ03LT_2
PHP_PHB_PHD66NQ03LT_2	20011210	Product data sheet	-	9397 750 09119	PHP_PHB_PHD66NQ03LT_1
PHP_PHB_PHD66NQ03LT_1	20011012	Product data sheet	-	9397 750 08725	-

9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

11. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

12. Trademarks

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

13. Contact information

For additional information, please visit: http://www.semiconductors.philips.com

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

14. Contents

Date of release: 2 August 2004

Document order number: 9397 750 13429

Published in The Netherlands